CLAIMS

1. A FET situated over a substrate, said FET comprising:

a channel situated in said substrate;

a first gate dielectric situated over said channel, said first gate dielectric having a first coefficient of thermal expansion;

a first gate electrode situated over said first gate dielectric, said first gate electrode having a second coefficient of thermal expansion;

wherein said second coefficient of thermal expansion is different than said first coefficient of thermal expansion so as to cause an increase in carrier mobility in said FET.

2. The FET of claim 1 wherein said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion.

3. The FET of claim 2 wherein said increase in said carrier mobility is caused by a tensile strain created in said channel.

4. The FET of claim 1 further comprising a second gate electrode situated between said first gate electrode and said first gate dielectric, said second gate electrode having a third coefficient of thermal expansion, said third coefficient of thermal expansion being greater than said first coefficient of thermal expansion and said third coefficient of thermal expansion being less than said second coefficient of

thermal expansion so as to cause a tensile strain in said channel, said tensile strain causing said increase in said carrier mobility.

5. The FET of claim 1 further comprising a second gate dielectric situated between said first gate dielectric and said substrate, said second gate dielectric having a third coefficient of thermal expansion, said third coefficient of thermal expansion being less than said first coefficient of thermal expansion and said second coefficient of thermal expansion being greater than said first coefficient of thermal expansion so as to cause a tensile strain in said channel, said tensile strain causing said increase in said carrier mobility.

6. The FET of claim 1 wherein said FET is a PFET.

7. The FET of claim 6 wherein said first coefficient of thermal expansion is greater than said second coefficient of thermal expansion so as to cause a compressive strain in said channel, said compressive strain causing said increase in said carrier mobility.

8. The FET of claim 1 further comprising a gate liner situated adjacent to said first gate dielectric and a gate spacer situated adjacent to said gate liner, said gate liner having a third coefficient of thermal expansion and said gate spacer having a fourth coefficient of thermal expansion, said fourth coefficient of thermal expansion

being greater than said third coefficient of thermal expansion so as to cause a tensile strain in said channel.

9. A FET situated over a substrate, said FET comprising a channel situated in said substrate, a first gate dielectric situated over said channel, said first gate dielectric having a first coefficient of thermal expansion, a first gate electrode situated over said first gate dielectric, said first gate electrode having a second coefficient of thermal expansion, said FET being characterized in that:

said second coefficient of thermal expansion being different than said first coefficient of thermal expansion so as to cause an increase in carrier mobility in said FET.

10. The FET of claim 9 wherein said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion so as to cause a tensile strain in said channel, said tensile strain causing said increase in said carrier mobility.

11. The FET of claim 9 further comprising a second gate electrode situated between said first gate electrode and said first gate dielectric, said second gate electrode having a third coefficient of thermal expansion, said third coefficient of thermal expansion being greater than said first coefficient of thermal expansion and said third coefficient of thermal expansion being less than said second coefficient of

thermal expansion so as to cause a tensile strain in said channel, said tensile strain causing said increase in said carrier mobility.

12. The FET of claim 9 further comprising a second gate dielectric situated between said first gate dielectric and said substrate, said second gate dielectric having a third coefficient of thermal expansion, said third coefficient of thermal expansion being less than said first coefficient of thermal expansion and said second coefficient of thermal expansion being greater than said first coefficient of thermal expansion so as to cause a tensile strain in said channel, said tensile strain causing said increase in said carrier mobility.

13. The FET of claim 9 wherein said FET is a PFET, said first coefficient of thermal expansion being greater than said second coefficient of thermal expansion so as to cause a compressive strain in said channel, said compressive strain causing said increase in said carrier mobility.

14. The FET of claim 9 further comprising a gate liner situated adjacent to said first gate dielectric and a gate spacer situated adjacent to said gate liner, said gate liner having a third coefficient of thermal expansion and said gate spacer having a fourth coefficient of thermal expansion, said fourth coefficient of thermal expansion being greater than said third coefficient of thermal expansion so as to cause a tensile strain in said channel.

15. A FET situated on a substrate, said FET comprising:

a channel situated in said substrate;

a gate stack situated over said channel;

a first gate dielectric situated in said gate stack, said first gate dielectric having a first coefficient of thermal expansion;

a first gate electrode situated over said first gate dielectric, said first gate electrode having a second coefficient of thermal expansion;

wherein said second coefficient of thermal expansion is different than said first coefficient of thermal expansion so as to cause a strain in said channel, said strain causing an increase in carrier mobility in said FET.

16. The FET of claim 15 wherein said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion so as to cause a tensile strain in said channel, said tensile strain causing said increase in said carrier mobility.

17. The FET of claim 15 further comprising a second gate electrode situated between said first gate electrode and said first gate dielectric, said second gate electrode having a third coefficient of thermal expansion, said third coefficient of thermal expansion being greater than said first coefficient of thermal expansion and said third coefficient of thermal expansion being less than said second coefficient of

thermal expansion so as to cause a tensile strain in said channel, said tensile strain causing said increase in said carrier mobility.

18. The FET of claim 15 further comprising a second gate dielectric situated between said first gate dielectric and said substrate, said second gate dielectric having a third coefficient of thermal expansion, said third coefficient of thermal expansion being less than said first coefficient of thermal expansion and said second coefficient of thermal expansion being greater than said first coefficient of thermal expansion so as to cause a tensile strain in said channel, said tensile strain causing said increase in said carrier mobility.

19. The FET of claim 15 wherein said FET is a PFET, said first coefficient of thermal expansion being greater than said second coefficient of thermal expansion so as to cause a compressive strain in said channel, said compressive strain causing said increase in said carrier mobility.

20. The FET of claim 9 further comprising a gate liner situated adjacent to said gate stack and a gate spacer situated adjacent to said gate liner, said gate liner having a third coefficient of thermal expansion and said gate spacer having a fourth coefficient of thermal expansion, said fourth coefficient of thermal expansion being greater than said third coefficient of thermal expansion so as to cause a tensile strain in said channel.